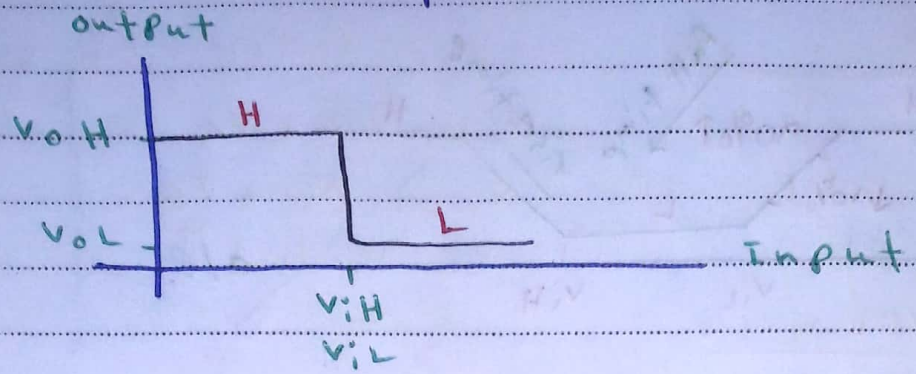
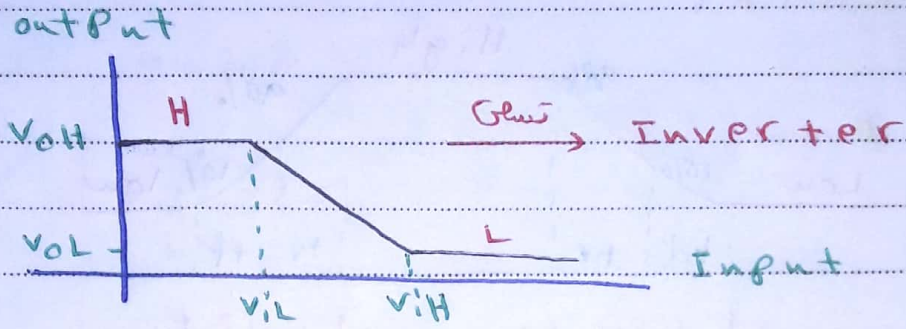
Subject: الكترونيات رقمية

بسم الله الرحمن الرحيم





↳ Voltage Input Low أكبر قيمة لـ Input يعتبر H

V_{TC} : Voltage Transfare characteristics

logic swing V_{LS} : $V_{oH} - V_{oL}$

transition width = $V_{TW} = V_{iH} - V_{iL}$

* Noise margin :

$V_{NMH} = V_{oH} - V_{iH}$

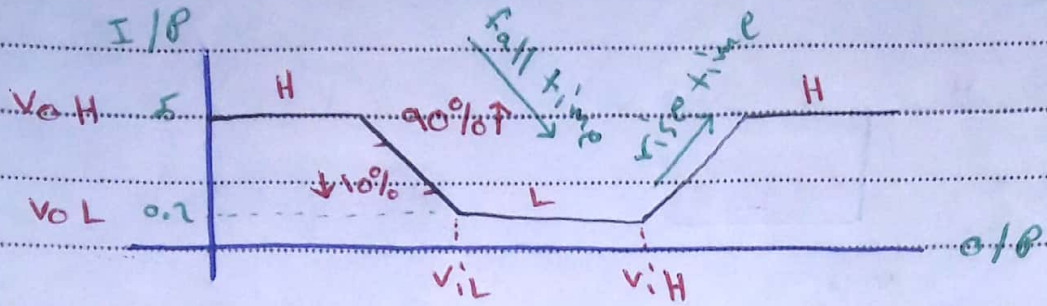
$V_{NML} = V_{iL} - V_{oL}$

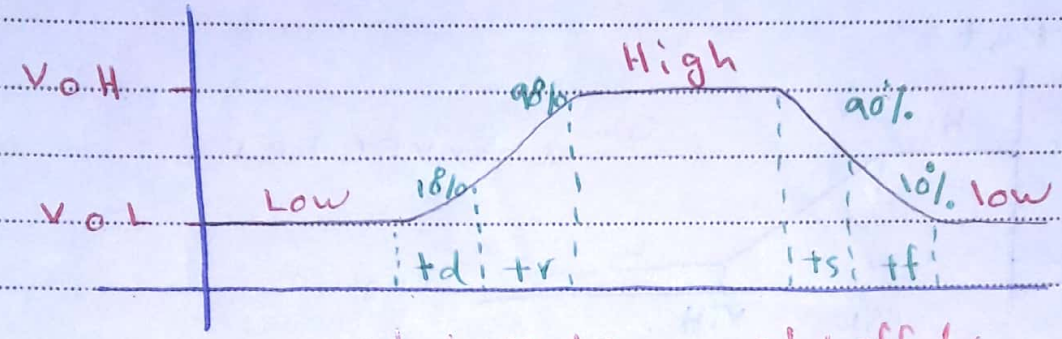
* Noise Immunity

$$V_{NIH} = \frac{V_{NMH}}{V_{LS}}$$

$$V_{NIL} = \frac{V_{NML}}{V_{LS}}$$

Subject:..... / /





→| ton |← →| toff |←

ton = td + tr

toff = ts + tf

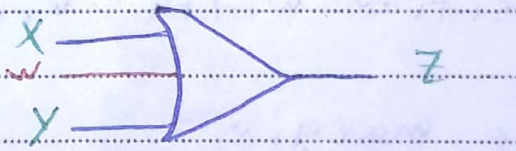
td : delay time

tr : rise time

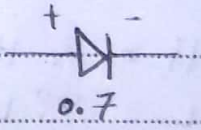
ts : storge time

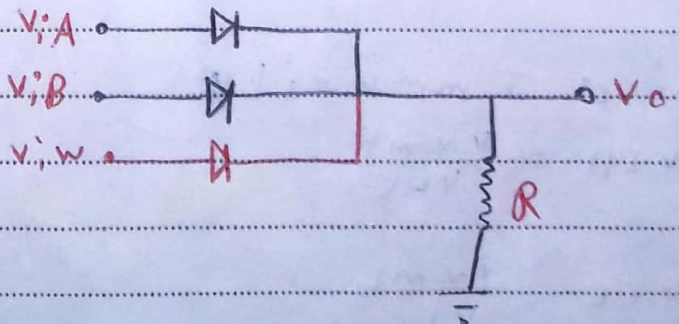
tf : fall time

OR - gate



X	Y	Z
L	L	L
L	H	H
H	L	H
H	H	H



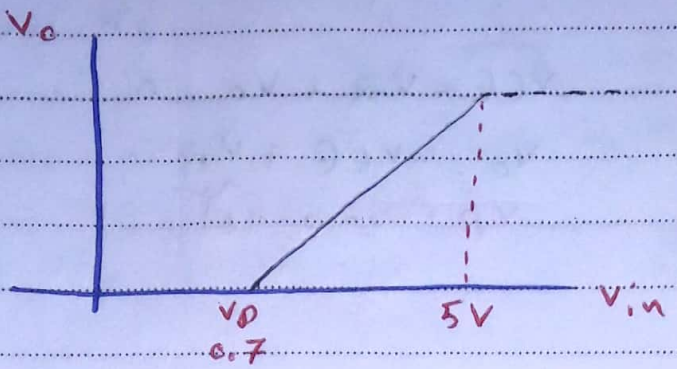


Vo A	Vo B	Vo
L	L	L
L	H	H $V_o = V_{iB} - 0.7$
H	L	H $V_o = V_{iA} - 0.7$
H	H	

L : V < 0.7

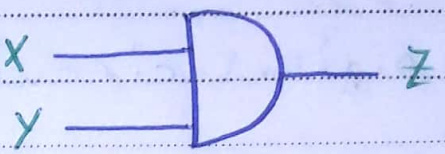
H : V ≥ 0.7

Subject:..... / /

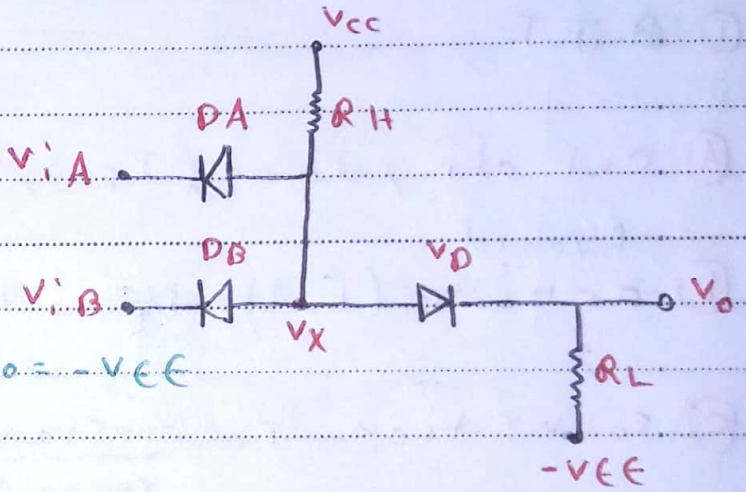


L : V < 0.7
H : V ≥ 0.7

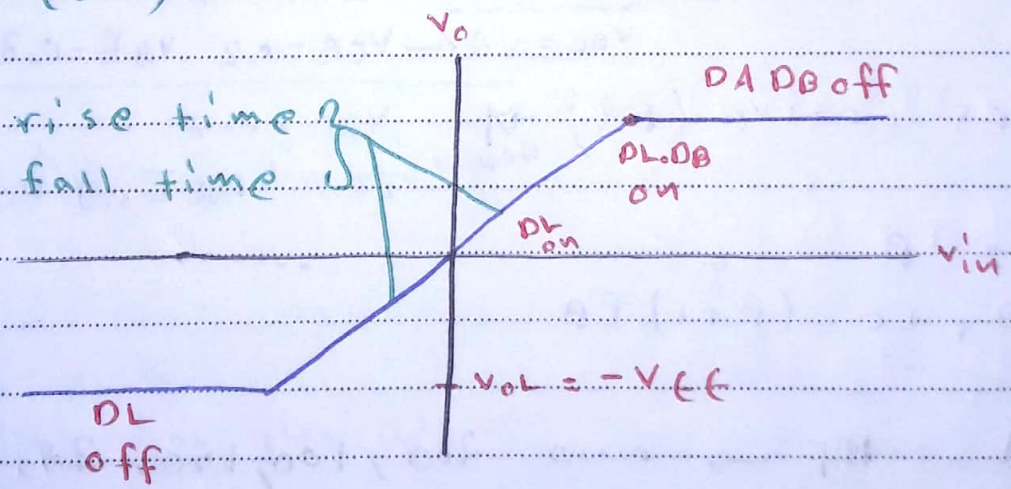
AND - gate

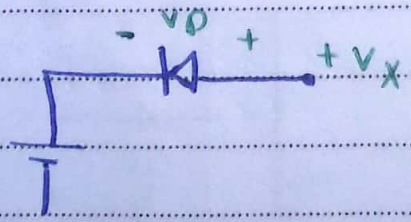


X	Y	Z
L	L	L
L	H	L
H	L	L
H	H	H



* DL (open) off => $V_o = -V_{EE}$
DL (ON)





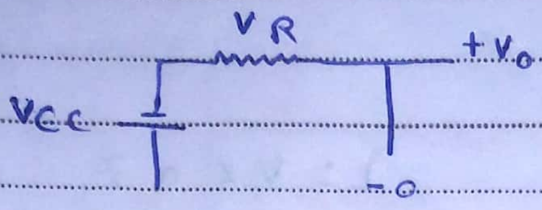
$V_X = V_i + V_{DB}$

$V_o = V_X - V_{DL}$

$V_o = V_i + V_{DB} - V_{DL}$

$V_o = V_i$

Subject: .... / /



$V_{CE} - V_R + V_o = 0$

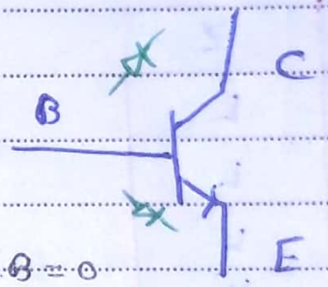
$V_o = -V_{CE} + V_R$

لازم نجد قيمة V_R

$$I = \frac{V_{CC} - V_{DL} + V_{EC}}{R_H + R_L}$$

ch 4 Digital circuit

① BJT



Ⓐ cut off , $I_C = 0$, $I_E = 0$, $I_B = 0$

forowid
Ⓑ active (F.A) off $V_{BE} = 0.7$

Ⓒ saturation I_C = constant = $\delta B_F I_B$ $I_B \uparrow$ $I_E \uparrow$

$V_{BC} = 0.6 \leftarrow V_{CE} = 0.2$ $V_{BE} = 0.8$ V

Ⓓ Revers active (RA) ON $V_{BC} = 0.7$

$I_E = -B_R I_B$ التيار بيخرج

$I_C = \beta \times I_B$

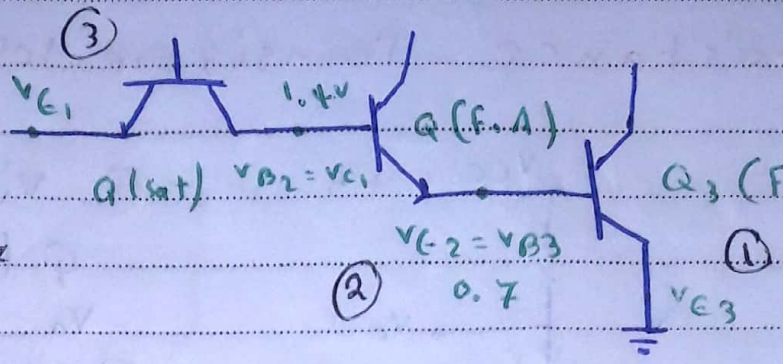
$I_E = I_B + I_C = (\beta + 1) I_B$

$0 < \delta < 1$ $B_F \rightarrow$ عالية 200, 100, 150, 25, 50

$B_R \rightarrow \approx 1$ range

Subject:..... / /

find V_{C1}



① $V_{BC_3} = 0.7$

$V_{B_3} - V_{E_3}^{0} = 0.7$

$V_{B_3} = 0.7$

② $V_{B_2} - V_{C_2} = 0.7$

$V_{B_2} = 0.7 + V_{E_2}$

$V_{B_2} = 0.7 + 0.7 = 1.4V$

③ $V_{CE_1} = 0.2$

$V_{C_1} - V_{C_1} = 0.2$

$V_{C_1} = V_{C_1} - 0.2$

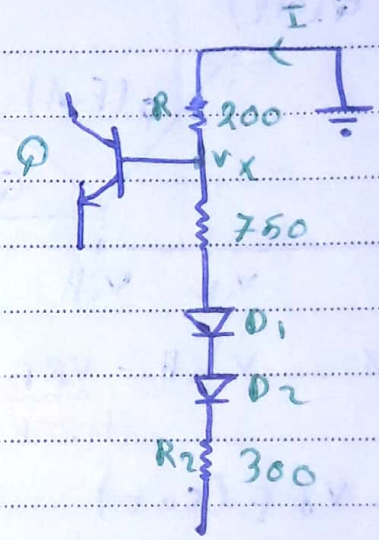
$V_{C_1} = 1.4 - 0.2 = 1.2V$

find I

$I_B \rightarrow mA \rightarrow$ يعمل لأنه قليل

$$I = \frac{V_{EE} - 2V_D}{R_1 + R_2 + R_3}$$

find V_{XB}



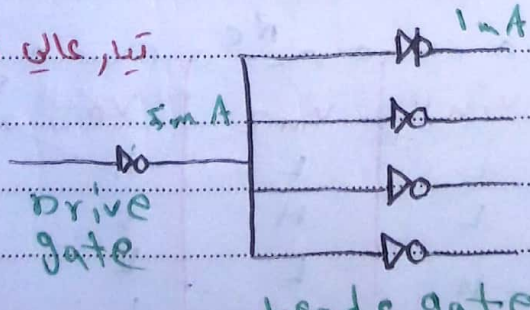
$-V_{EE} = -5.2$ Volt

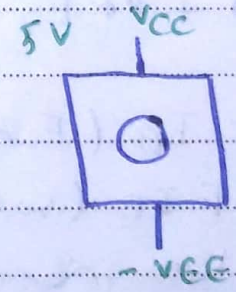
Design family

1. power Dissipation
2. fan-out

تيار قليل أفضل

تيار عالي أفضل





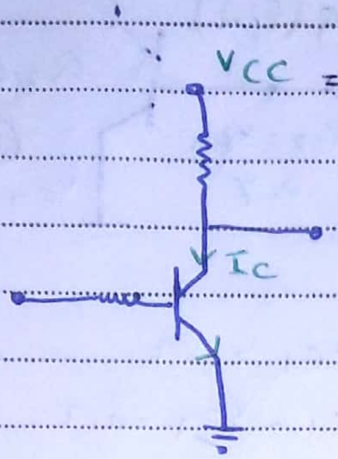
fan-out : loads gates

تيار تحمل

Drive gate

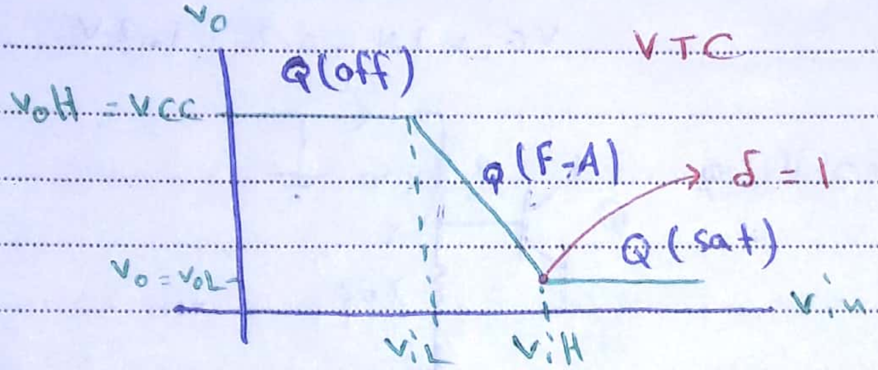
Subject: .... / /

Resistance - Transistor logic (RTL)

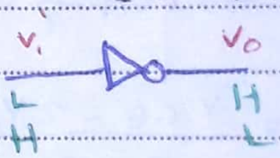


① Vin Low
Q (off)
$V_o = V_{CC}$ (V_{oH})

② Vin High
Q (sat)
$V_o = V_{CE}(sat) = 0.2$



يعمل هذا الشكل
Inverter



$V_{iL} = 0.7$ $V_{inH} = V_{RB} + V_{BE}(sat)$

عشان ي (sat)

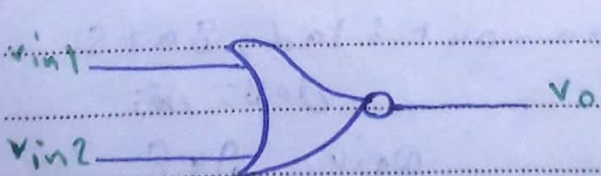
$= I_B R_B + V_{BE}(sat)$

$= \frac{I_C}{\beta_F} R_B + V_{BE, sat}$ → 0.8

$I_C = \beta_F I_B$ (F.A)

$I_C = \delta \beta_F I_B$ (sat) $= I_C = \frac{V_{CC} - V_{CE}(sat)}{R_C}$

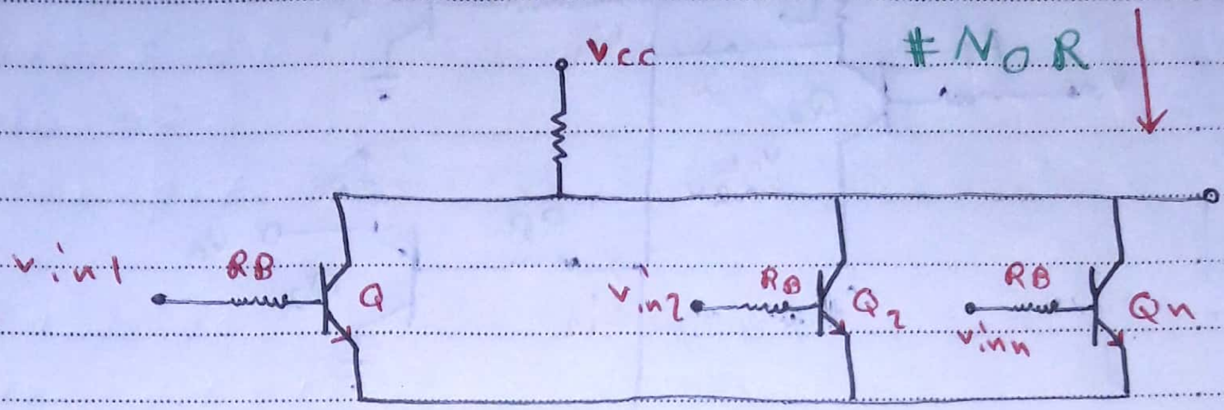
NOR gate



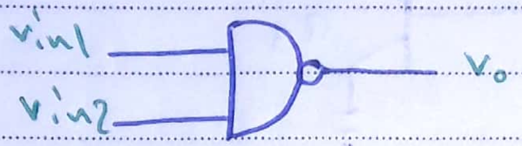
vin1	vin2	Vo
L	L	H → sat
L	H	L
H	L	L
H	H	L

L: off (Q)   H: sat (Q)

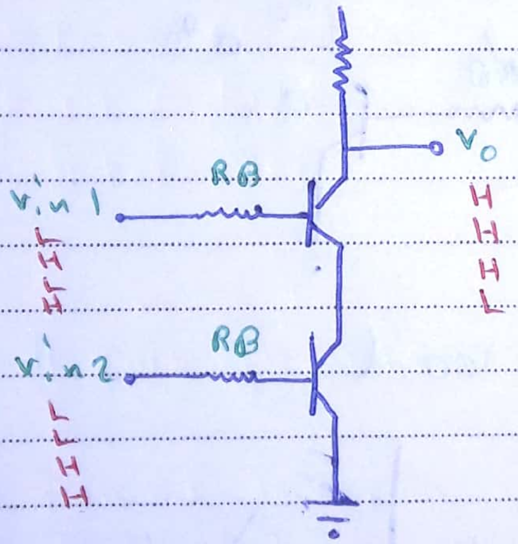
NOR



NAND gate



vin1	vin2	Vo
L	L	H
H	L	H
L	H	H
H	H	L



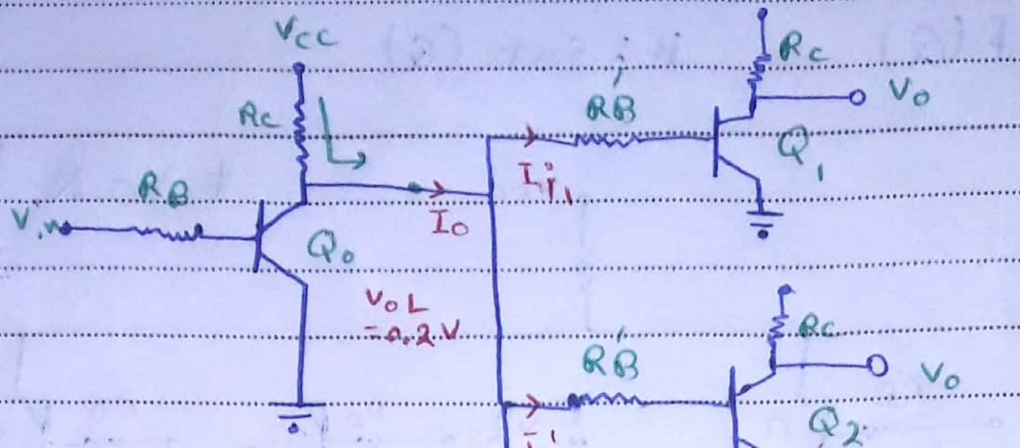
Note: إذا أدخلنا أداة Not على الـ Vo نحصل على AND

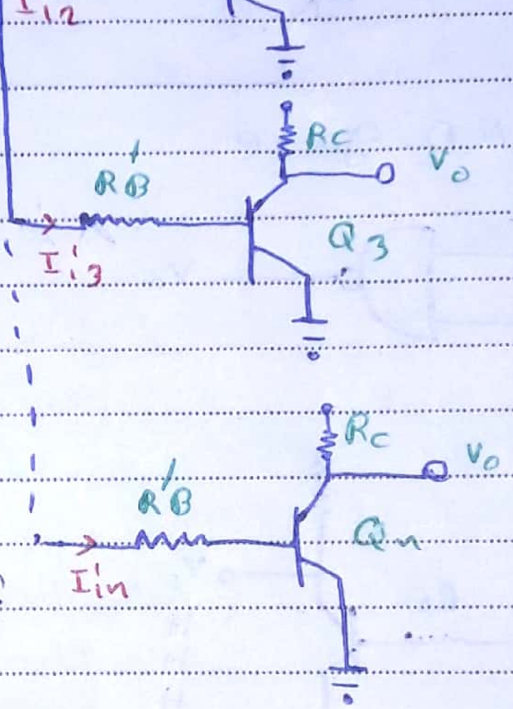
$V_C = (V_{CE_1} + V_{CE_2})\ sat$

$= 0.2 + 0.2 = 0.4$

$V_o = \sum_{n=1}^{n} 0.2 = 0.2 * n$

Subject: .... Same / /





①

$V_{oL} = 0.2$

وهذا غير كافي لتشغيل أي Qs

لذلك ننشغل بالحالة (H)

②

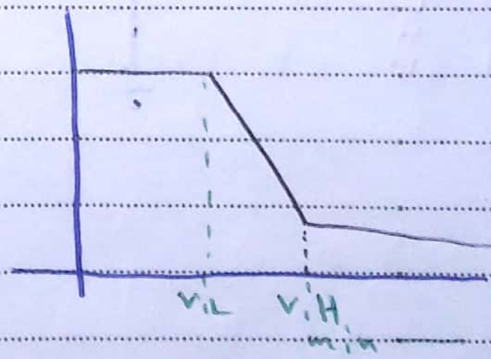
$V_{oH} = V$

$N = \frac{I_{oH}}{I_i}$ $Q_o = off$

$I_{oH} = I_{Rc} = \frac{V_{cc} - V_{oH}}{R_c}$

load

$I_i = I'_{B} = \frac{V_{oH} - V_{BE(sat)}}{R'_B}$



$V_{oH} = V_{iH\,min} = I'_b R'_B + V_{BE(sat)}$

$= \frac{I'_c}{\beta_f} R'_B + V_{BE(sat)}$

$V_{oH} = V_{iH\,min} = \frac{V_{cc} - V_{CE(sat)}}{\beta_f\, R_c} \cdot R'_B + V_{BE(sat)}$

Subject:..... / /

$R_B = 10K\ \Omega$

$R_C = 1K\ \Omega$

$V_{CC} = 5\ V$

$\beta_f = 25$

$V_{oH} = \frac{5 - 0.2}{25.1K} \cdot 10K + 0.8 = 2.7\ V$

$I_{oH} = \frac{5 - 2.7}{1K} = 2.3\ mA$

$I_i' = \frac{2.7 - 0.8}{10K} = 0.19\ mA$

$N = \frac{I_o}{I_i} = \frac{2.3\ m}{0.19\ m} = 12.19 = 12$